**[Programmable Communication Group](https://sites.google.com/a/temple.edu/programmable-communication-group/)**

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| Date | Friday, October 4, 2013 | | |
| Advisor | Dr. Silage | | |
| Members | Cedric Destin | Brandon Keith | Brian Thibodeau |

Headline: Website posting due today (10/07/13) and Monday, 10/21/13. Draft Design document due 10/18/13. Second WebEx project review due 10/18/13.

Topics to discuss (with Silage)

* Who should be able to view the WebEx project reviews?
* Preliminary Simulink simulation of 2nd-order Costas loop.

**TBD**

Topics to discuss (among SD team and Silage, if necessary)

* Who on the team will prepare next WebEx design review for 10/21/13?
* Should Cedric implement FSK in simulation of KD2BD transmitter?

Dr. Silage feedback

* The modem specification sheet that was uploaded to GitHub (“demo\_modem\_spec\_sheet.pdf”) is for an RF modem, not a baseband modem.
* Be mindful of Keplerian elements for Doppler shift.

**TBD**

Topics to discuss in next SD meeting

* Implementing PLL in FPGA (besides from Costas loop).
  + A standard PLL can be implemented using a multipier (phase detector), FIR filter (Loop filter) and a DDS (VCO). Unless Xilinx provides a logicCore block of a PLL.
  + Are they any other ways of performing symbol and timing recovery that may be a more efficient hardware implementation that wouldn’t require a PLL?

**TBD**

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| **Engineer** | **Status** |
| Brian Thibodeau | * Evaluating and testing transfer function that I believe correctly models the Costas loop. Once this model is confirmed to behave as the simulation, the transfer function can be tuned to meet the specifications of our modem. This includes the ability to track and lock onto Doppler shift * Determining need requirements for the Costas loop:   + Costas Loop BW   + Filter BWs   + Keplarian elements for determination of specific Doppler shift needs. (time, frequency range) * Need research into AGC implementation.   + A time varying gain of the input signal to the Costas loop will interfere with the gains of the Costas loop that determine settling time, steady state error, etc. |
| Cedric Destin |  |
| Brandon Keith | * 1st WebEx project review video completed * Working on draft design documentation * Defining specifications for final deliverable(s) * Would like a sample-based Simulink implementation |